BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1 through 16 remain in this case. Claims 1 through 3 and 13 are amended.

The Examiner objected to claim 13 as having an informality relative to the "inhibit" phrase. Claim 13 is amended as suggested by the Examiner[1], overcoming the objection.

The undersigned notes the objection to claim 13 as dependent on a rejected claim, but otherwise directed to patentable subject matter. Claim 13 is amended to be in independent form, including the limitations of the claims upon which it previously depended. Allowance of claim 13 is therefore respectfully requested.

Claims 1 and 3 were rejected under §112, ¶2, as indefinite for failing to particularly point out and distinctly claim the subject matter of the invention.

Regarding claim 1, the Examiner found the phrase "the modification tracking circuitry operable to inhibit a redundant fetch of the operand" to be unclear as being subject to two possible meanings, one of which the Examiner found to be inoperable. The Examiner posits that the phrase may refer to a conditional inhibition of the fetch (with an unstated condition) or to an unconditional inhibition of the fetch, in which case the invention would be inoperable because no fetches could occur.

Applicants respectfully traverse the §112 rejection of claim 1. The objected-to phrase in the claim does not refer to the inhibiting of any and all operand fetches, but only to the inhibiting of *redundant* fetches of operands. Whether this inhibiting is subject to a further condition (*i.e.*, beyond the implicit condition that the fetch being inhibited is redundant) is not relevant to this claim, nor does the operability of the invention depend on whether a further condition exists. If the inhibiting is otherwise unconditional, the invention remains operable

[1] Office Action of March 29, 2004, page 3, ¶7a.

because the first operand fetch (*i.e.*, the previous fetch that renders a subsequent fetch redundant) has already fetched the operand, and this operand can be used in execution. Accordingly, Applicants respectfully submit that the indefiniteness asserted by the Examiner does not in fact exist in the claim as written, and that claim 1 is sufficiently definite to meet the requirements of §112, ¶2.

Claim 1 is also amended, as will be discussed in further detail below relative to the prior art rejection, to recite that the inhibiting of the redundant fetch is performed responsive to the contents of the address pointer circuitry not being modified since a previous memory access using the contents of the address pointer circuitry. The specification clearly supports this amendment to claim 1,[2] and as such no new matter is presented by this amendment. Applicants further respectfully submit that this amendment to claim 1 further clarifies the modification tracking circuitry element, which the Examiner found unclear, by providing this additional responsive action of the inhibiting.

Withdrawal of the §112 rejection of amended claim 1 is respectfully requested.

Claim 3 was rejected under §112, ¶2 as indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. The Examiner asserted that the phrase "stand alone coefficient data pointer", because it was unclear what it was that the coefficient data pointer stood alone from.[3] Claim 3 is amended to overcome the rejection by canceling the "stand alone" phrase, and to more concisely clarify that the address pointer circuitry comprises the recited coefficient data pointer. Applicants respectfully submit that amended claim 3 overcomes the §112 rejection, and withdrawal of the §112 rejection of claim 3 is respectfully urged.

Claims 1 through 3 and 9 through 12 were rejected under §102(a) as unpatentable over the Widigen et al. reference[4]. The Examiner asserted that the Widigen et al. reference teaches all of the elements of these claims, including the inhibiting of a redundant fetch of an operand,

---

[2] *See* specification of S.N. 09/716,493, at page 22, lines 18 through 24.
[3] Office Action, *supra*, page 4, ¶11.
[4] U.S. Patent No. 5,919,256, issued July 6, 1999 to Widigen et al., from an application filed March 26, 1996.

which the Examiner found to be disclosed by the description of the operand cache of the reference.[5]

Claims 4 and 14 through 16 were rejected under §103 as unpatentable over the Widigen et al. reference, as applied against the independent claims 1 and 9, in view of the Touriguian et al. reference[6]. The Examiner found that the Widigen et al. reference does not teach a multiple-accumulate unit as an execution unit, but that the Touriguian et al. reference teaches such a unit, and that it would have been obvious to combine that multiple-accumulate unit into the Widigen et al. system to efficiently execute digital signal processing instructions.[7] These claims were rejected accordingly.

Claim 5 was rejected under §103 as unpatentable over the Widigen et al. reference as applied to claim 1, in view of the Schacham et al. reference[8]. The Examiner found that the Widigen et al. reference does not teach a touch instruction "mar(*CDP)" to flag that the operand has been updated and can now be fetched, but that the Schacham et al. reference discloses such an operation in connection with its cache invalidation instruction, which forces the operand to be re-fetched. The Examiner found that it would have been obvious to combine these teachings to ensure that the correct data is available for execution, and rejected claim 5 accordingly.[9]

Claim 6 was rejected under §103 as unpatentable over the Widigen et al. reference as applied to claim 1, in view of the Okabayashi et al. reference[10]. The Examiner found that the Widigen et al. reference does not disclose an override mechanism to disable the modification tracking circuitry, but that such a mechanism is disclosed by the Okabayashi et al. reference in connection with its disabling of cache circuitry during a debugging mode. The Examiner found that it would have been obvious to modify the Widigen et al. teachings with those of the

---

[5] Office Action, *supra*, page 5, ¶14d; page 6, ¶17c (*citing* the Widigen et al. reference at column 8, lines 7 through 27).
[6] U.S. Patent No. 5,832,257, issued November 8, 1998 to Touriguian et al.
[7] Office Action, *supra*, pages 8 and 9, ¶¶ 21 through 28.
[8] Published U.K. Patent Application GB220481A, published August 3, 1998.
[9] Office Action, *supra*, page 10, ¶ 31.
[10] U.S. Patent No. 6,505,309, issued January 7, 2003 to Okabayashi et al., from an application filed March 19, 1999.

Okabayashi et al. reference so that problems could be more accurately located.[11] Claim 6 was rejected accordingly.

Claim 7 was rejected under §103 as unpatentable over the Widigen et al. reference as applied to claim 1, in view of the Salem et al. reference[12]. The Examiner found that the Widigen et al. reference does not disclose that the modification tracking circuit is operable to only track address pointer modification during looping operations of the execution unit, but that the Salem et al. reference discloses the inhibition of fetching to a cache from memory during looping operations to save power, and that it would have been obvious to modify the Widigen et al. reference according to these teachings for the same reason.[13] Claim 7 was rejected accordingly.

Claim 8 was rejected under §103 as unpatentable over the Widigen et al. reference as applied to claim 1, in view of the Willkie et al. reference[14]. The Examiner found that the Widigen et al. reference did not disclose that the digital system of the claim was a cellular telephone, but that such a telephone, into which the system of Widigen et al. could be obviously combined, is disclosed by the Willkie et al. reference.[15]

Claim 1 is amended to overcome the rejection. As discussed above, claim 1 is amended to recite that the modification tracking circuitry inhibits the redundant fetch of the operand in response to the contents of the address pointer circuitry not being modified since a previous memory access using its contents. This responsive operation of the modification tracking circuitry provides a processor or DSP architecture in which high code density and easy programming can be attained, particularly in minimizing coefficient fetches from memory without undue overhead.

Claim 2, dependent on claim 1, is amended for clarity.

---

[11] Office Action, *supra*, page 10, ¶ 34.
[12] U.S. Patent No. 5,623,615, issued April 22, 1997 to Salem et al.
[13] Office Action, *supra*, page 11, ¶ 37.
[14] U.S. Patent No. 5,923,705, issued to July 13, 1999 to Willkie et al.
[15] Office Action, *supra*, pages 11 and 12, ¶¶ 40 and 41.

Applicants respectfully submit that claim 1 is novel and patentably distinct over the Widigen et al. reference and the other prior art of record in this case.

Applicants submit that the Widigen et al. reference fails to disclose the modification tracking circuitry of the claim, recited in claim 1 as operable to inhibit a redundant fetch of the operand responsive to the contents of the address pointer circuitry not being modified since a previous access using those contents.

As mentioned above, the Examiner asserts that the Widigen et al. reference teaches the inhibiting of a redundant fetch of the operand because (i) if an operand is not in the operand cache, the operand has to be fetched from memory, and (ii) if the operand is in the operand cache, that operand from the cache is sent to the execution unit.[16] But these teachings do not ensure that redundant fetches are inhibited. In fact, the Widigen et al. reference goes on to disclose that a subsequent fetch from memory is *required* even if the operand is in the operand cache. According to the reference, when the operand is provided from its operand cache, execution of the operation "can proceed immediately on a speculative basis",[17] and that the two tasks of calculating the operand address and retrieving the operand from that address "are still required in order to verify the correctness of the cached operand".[18] In other words, according to the Widigen et al. reference, a redundant fetch is performed to confirm that the value of the operand in the operand cache was correct.[19] According to this disclosed operation of the Widigen et al. system, there is no inhibiting of redundant operand fetches whatsoever.

The Widigen et al. reference goes on to say that, in the alternative to the fetching and confirming of the value of the operand, that consistency between the operand cache and memory may be maintained so that the correctness of the cached operand need not be verified.[20] However, there is no disclosure, in the reference, of how this consistency is to be attained. One can only surmise that conventional cache operations (maintaining "dirty" bits, or effecting

---

[16] Office Action, *supra*, page 5, ¶ 14d.
[17] Widigen et al., *supra*, column 8, lines 32 through 34.
[18] Widigen et al., *supra*, column 8, lines 34 through 39.
[19] Widigen et al., *supra*, column 8, lines 36 through 39.
[20] Widigen et al., *supra*, column 8, lines 39 through 42.

"write-through" or "write-back" operations) are used. But there is no disclosure nor suggestion, even from this portion of the Widigen et al. reference referring to this alternative implementation, of any circuitry that determines whether the contents of address pointer circuitry were not modified since a previous memory access using those contents, and inhibiting an operand fetch in response to that state, as now required by amended claim 1.

Accordingly, Applicants respectfully submit that amended claim 1 and its dependent claims are all novel over the Widigen et al. reference.

Applicants further submit that amended claim 1 and all of its dependent claims are patentably distinct over the prior art of record in this case, on the grounds that the combined teachings of this prior art falls short of the requirements of amended claim 1, and that there is no suggestion from the prior art to modify these teachings so as to reach the claim.

As noted above, there is no disclosure from the Widigen et al. reference of the modification tracking circuitry required by amended claim 1, particularly its operation in response to the contents of the address pointer circuitry not being modified since a previous memory access using the contents of the address pointer circuitry. None of the other applied references add any teachings in this regard. At best, while the Examiner asserted that the Salem et al. reference discloses the inhibition of fetching to a cache from memory during looping operations to save power, there is no disclosure by that reference of the inhibiting of operand fetching responsive to the contents of the address pointer circuitry not being modified since a previous memory access using those contents, as required by amended claim 1. The other applied references indeed are in no way directed to this feature. Accordingly, the combined teachings of the applied references fall short of the requirements of amended claim 1.

Applicants further respectfully submit that there is no suggestion from the prior art to modify these teachings in such a manner as to reach amended claim 1. As discussed above, the Widigen et al. reference teaches either actually performing the redundant operand fetch to verify that the cached operand was correct, or maintaining cache coherency to ensure that the operand cache is correct. There is no suggestion from this reference, nor from the other

references, of examining the contents of an address pointer that was used to fetch the operand, to determine whether those contents have been modified, in order to make this decision. The elegant way of saving memory fetches provided by the invention of amended claim 1 and its dependent claims is not only the difference between the claim and the prior art, but is also the source of the important advantages provided by this invention, further supporting the patentability of these claims.

For these reasons, Applicants respectfully submit that amended claim 1 and its dependent claims are patentably distinct over the prior art of record in this case.

Applicants also respectfully traverse the §102 rejection of claims 9 through 11, as anticipated by the Widigen et al. reference.

Independent method claim 9 requires, among other steps, the step of executing a second instruction by inhibiting the fetching of a second operand from memory if the data pointer, which was loaded with a first address value used to fetch a first operand from memory in a first instruction, has not been modified since the executing of the first instruction. Applicants submit that the Widigen et al. reference lacks any teachings in this regard.

As discussed above relative to amended claim 1, the Widigen et al. reference teaches that, if an operand is present in an operand cache and is provided to a processor, either a redundant fetch of that operand from memory is "required in order to verify the correctness of the cached operand",[21] or alternatively consistency between the operand cache and memory must be maintained (in which case verification of the cached operand need not occur).[22] In other words, contrary to the assertion by the Examiner, the mere fact that the operand cache provides an operand to a processor does not necessarily mean that a redundant fetch is inhibited. But in any case, there is no disclosure in the Widigen et al. reference of the inhibiting fetching of an operand from memory based on whether the data pointer that was loaded with an address value for a first operand has or has not been modified since the first operand was

---

[21] Widigen et al., *supra*, column 8, lines 34 through 39.
[22] Widigen et al., *supra*, column 8, lines 39 through 42.

fetched, as required by claim 9. Accordingly, Applicants respectfully submit that the teachings of the Widigen et al. reference fall short of the requirements of claim 9.

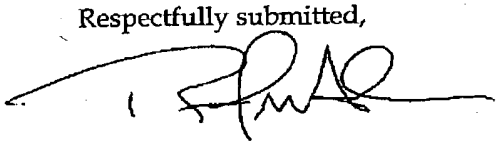
For this reason, Applicants submit that claim 9 and its dependent claims 10 and 11 are novel over the Widigen et al. reference, and accordingly traverse the §102 rejection of these claims.

For similar reasons as discussed above, Applicants submit that claims 9 through 11 are patentably distinct over the prior art of record in this case.

None of the secondary references applied against the apparatus claims provide any teachings regarding the inhibiting of the fetching of an operand from memory if the data pointer, which was loaded with a first address value used to fetch a first operand from memory in a first instruction, has not been modified since the executing of the first instruction, as required by claim 9 and which is absent from the teachings of the Widigen et al. reference. And also as discussed above, Applicants submit that there is no suggestion from the prior art to modify these teachings to reach the claim, especially considering that none of the references in any way mention or discuss monitoring of an address used to fetch a first operand, much less in order to avoid a redundant fetch of that operand if the address has not changed by the time of a second fetch. Especially considering the important advantages provided by this difference between the claims and the prior art, Applicants therefore respectfully submit that claims 9 through 11 are not only novel over the prior art, as urged above, but indeed are patentably distinct over this art.

For these reasons, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of this application is therefore respectfully requested.

Respectfully submitted,

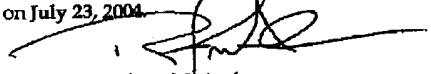


Rodney M. Anderson
Registry No. 31,939
Attorney for Applicants

Anderson, Levine & Lintel, L.L.P.
14785 Preston Road, Suite 650
Dallas, Texas 75254
(972) 664-9554

CERTIFICATE OF FACSIMILE TRANSMISSION
37 C.F.R. 1.8

The undersigned hereby certifies that this correspondence is being facsimile transmitted to the Patent and Trademark Office (Fax Number 703-872-9306) on July 23, 2004.



Rodney M. Anderson
Registry No. 31,939